# BK7259 Datasheet

DS-BK7259-E02 V1.1

2025/2/14

# Contents

# 1. Features

## Wi-Fi®

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20/40 MHz channel bandwidth for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- TX and RX Low-Density Parity Check (LDPC) support for extended range
- WPA/WPA2/WPA3-Personal support for enhanced security
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- TX power up to +20 dBm
- RX sensitivity -98 dBm

## Bluetooth®

- Dual-mode Bluetooth 5.4 compliant
- Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2 Mbps and 3 Mbps, Low Energy (LE) 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE Audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

## Dual Cores

- Dual Arm®v8.1-M Cortex®-M52 MCUs at up to 480 MHz
  - Arm Helium™ vector processing enables enhanced DSP and machine learning (ML) processing
  - Half-, full-, and double-precision floating-point unit (FPU)
  - Arm TrustZone® for system-wide security and protection of software investments
  - PACBTI extension (Pointer Authentication, Branch Target Identification) mitigated SW ROP/JOP attacks
- UART flash download
- Serial Wire Debug (SWD) interface
- UART for debugging

## Memories

- 8 MB SiP flash
- SiP PSRAM: up to 32 MB
- 1.152 MB RAM
- 128 KB ROM
- eFuse

## Clock Management

- External oscillators: 26 MHz crystal oscillator (XTALH), 32 kHz crystal oscillator (XTALL)
- Internal oscillators: 160–640 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 960 MHz PLL (DPLL)
- 90–99 MHz audio PLL (APLL)

## Power Management

- 2.3 to 3.6 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converters and LDO regulators
- Low power consumption:
  - Active mode RX: 18 mA
  - Sleep mode: 43 µA
  - Deep sleep mode: 16 µA
  - Shutdown mode: 3 µA
  - DTIM10 mode: 80 µA

## Peripherals

- 64 GPIOs
- 3x SPI interface (SPI)
- 2x QSPI interface (QSPI)
- 5x UART interface (UART)
  - 1 supports hardware flow control and flash download support
  - 1 supports CPU core debugging
- 1x Smart Card controller (SC)
- 2x SD/SDIO and eMMC host controller (SDMMC)
- 4x I2C interface (I2C)

- 1x I3C interface (I3C)
- 1x high-speed USB2.0 (HS) (USB)
- 1x CAN controller with CAN FD (CAN)
- 1x LIN controller (LIN)
- 1x general-purpose DMA controller (GDMA) with 8 channels
- 1x high-performance DMA controller (HPDMA) with 8 channels
- 1x Ethernet MAC interface (ENET)
- 12x 32-bit PWM channel
- Video
  - 1x display controller (DISPLAY)
  - 1x MIPI® DSI, 4 data lanes, up to 1.5 Gbps each
  - 1x 10-bit DVP interface
  - 1x MIPI® CSI, 2 data lanes, up to 1.5 Gbps each
  - 1x image signal processor (ISP)
  - 1x video processing unit (VPU)
  - 1x graphics processing unit (GPU)
  - 1x display processor unit (DPU)
- Audio
  - 1x 20-band digital hardware equalizer (EQ)
  - 3x audio ADC
  - 2x audio DAC
  - 2x DMIC interface (DMIC)
  - 2x SPDIF interface (SPDIF)
  - 1x HDMI CEC controller (HDMI CEC)
  - 4x I2S interface (I2S)
- 12-bit AUX ADC, up to 11 channels
- 12x 32-bit general-purpose timer
- 1x AON watchdog timer (AWDT)
- 2x CPU window watchdog timer (WWDT)
- 1x real-time counter (RTC)
- 1x IrDA Interface (IRDA)
- 1x temperature sensor

## Packaging

- QFN128 package, 12.3 x 12.3 mm
- Operating temperature range: -40 to +85 °C

## Applications

- Smart door lock with large visual screen
- IP video intercom
- Digital picture frame
- AoV (Always on Video) IP camera
- HMI (Human Machine Interface) application
- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor

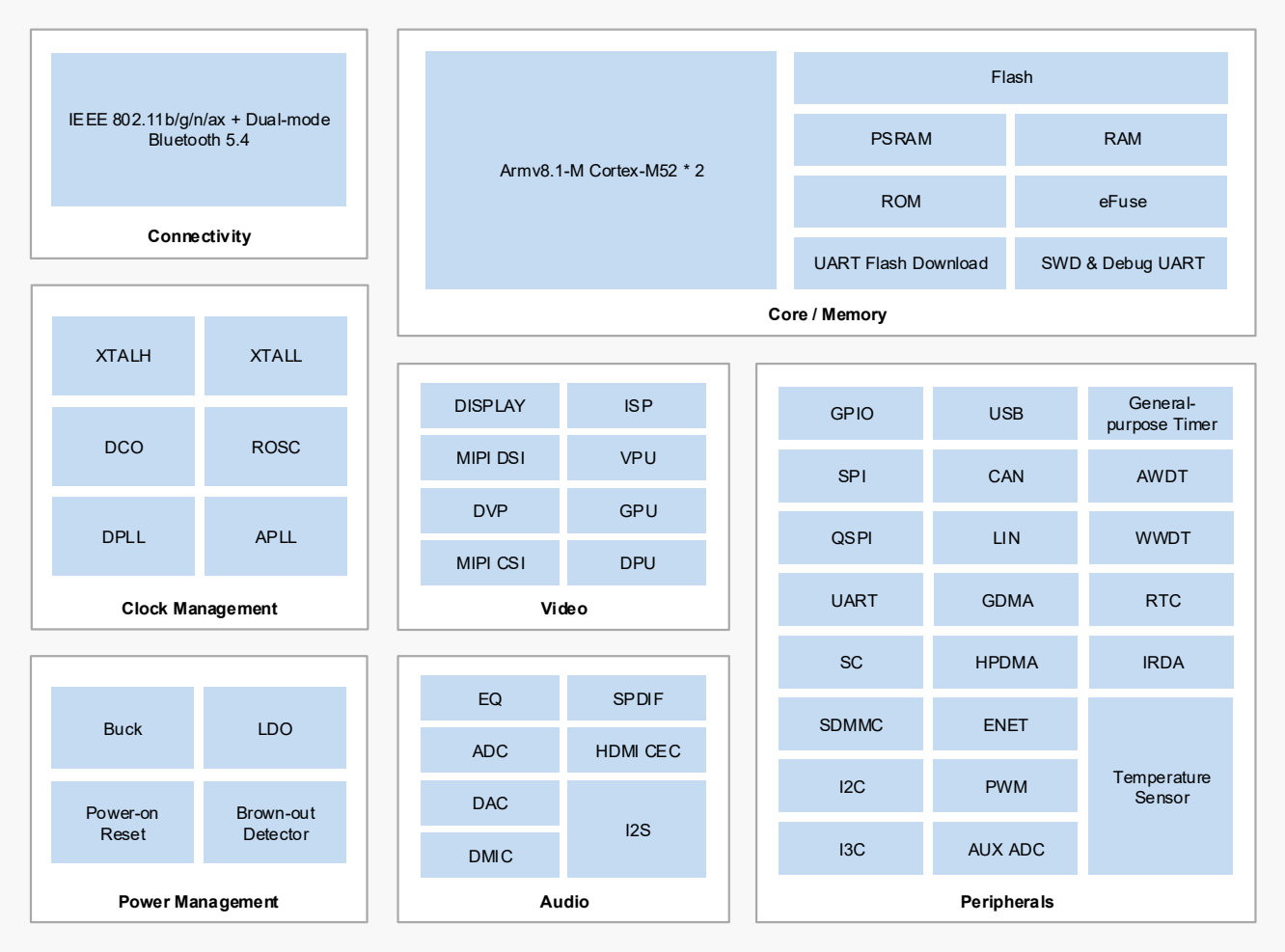
# 2. Overview

The BK7259 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and dual-mode Bluetooth 5.4 combo solution designed for applications that require abundant resources and low power consumption. The integration of dual Armv8.1-M Cortex-M52 MCUs and a comprehensive set of peripherals makes the BK7259 ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and ultra-low power process technology, the BK7259 delivers high integration and minimal power consumption for smart door locks with large visual screens, IP video intercoms, digital picture frames, AoV IP cameras, HMI applications, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of the BK7259.

**Figure 2-1 BK7259 Block Diagram**



# 3. Pin Descriptions

The BK7259 provides Wi-Fi and Bluetooth functionality in a 12.3 x 12.3 mm, 128-pin QFN package.

## 3.1 QFN128 Pin Descriptions

Figure 3-1 shows the pin assignments of the QFN128 package.

**Figure 3-1 QFN128 Pin Assignments**

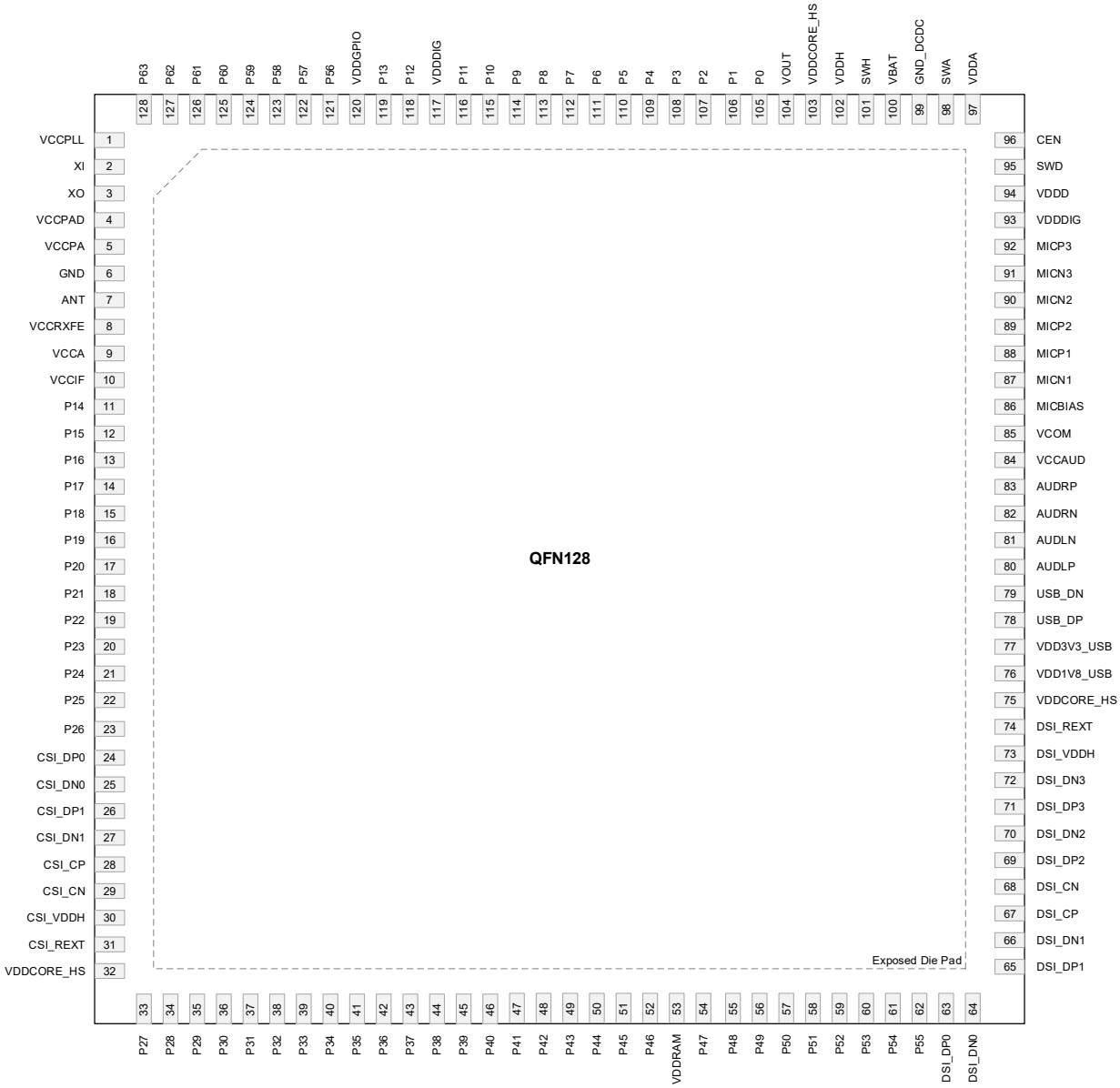


Table 3-1 shows the pin descriptions of the QFN128 package.

**Table 3-1 QFN128 Pin Descriptions**

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 1 | VCCPLL | - | Analog input | RF PLL power supply |
| 2 | XI | - | Analog input | 26 MHz crystal input |
| 3 | XO | - | Analog output | 26 MHz crystal output |
| 4 | VCCPAD | - | Analog input | RF PA driver power supply |
| 5 | VCCPA | - | Analog input | RF PA power supply |
| 6 | GND | - | GND | Ground |
| 7 | ANT | - | RF | 2.4 GHz RF signal port |
| 8 | VCCRXFE | - | Analog input | RF receiver power supply |
| 9 | VCCA | - | Analog input | Analog power supply |
| 10 | VCCIF | - | Analog input | IF power supply |
| 11 | P14 | I/O | Digital | • GPIO14: general-purpose I/O<br>• BT_ANT0: Bluetooth antenna select<br>• SD1_CLK: clock<br>• RGB_DE: data enable<br>• ENET_TXD3: transmit data |
| 12 | P15 | I/O | Digital | • GPIO15: general-purpose I/O<br>• BT_ANT1: Bluetooth antenna select<br>• SD1_CMD: command/response<br>• RGB_VSYNC: vertical synchronization<br>• ENET_TXD2: transmit data |
| 13 | P16 | I/O | Digital | • GPIO16: general-purpose I/O<br>• BT_ANT2: Bluetooth antenna select<br>• SD1_DATA0: data<br>• RGB_HSYNC: horizontal synchronization<br>• ENET_TXD1: transmit data |
| 14 | P17 | I/O | Digital | • GPIO17: general-purpose I/O<br>• BT_ANT3: Bluetooth antenna select<br>• SD1_DATA1: data<br>• RGB_DISP: display on enable |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • ENET_TXD0: transmit data |
| 15 | P18 | I/O | Digital | • GPIO18: general-purpose I/O<br>• SD1_DATA2: data<br>• RGB_DCLK: clock output<br>• CLK_AUXS_ENET: reference clock for external Ethernet PHY, derived from DCO/APLL |
| 16 | P19 | I/O | Digital | • GPIO19: general-purpose I/O<br>• SD1_DATA3: data<br>• RGB_B7: blue data<br>• ENET_MDC: management data clock |
| 17 | P20 | I/O | Digital | • GPIO20: general-purpose I/O<br>• SD1_DATA4: data<br>• RGB_B6: blue data<br>• ENET_MDIO: management data<br>• EXT_FLASH_CSN: external flash chip select<br>• CPU_SWCLK: serial wire clock |
| 18 | P21 | I/O | Digital/Analog | • GPIO21: general-purpose I/O<br>• SD1_DATA5: data<br>• ENET_REF_CLK: RMII reference clock<br>• RGB_B5: blue data<br>• ENET_GRCLK: RGMII timing reference for RX data transfers<br>• EXT_FLASH_SCK: external flash clock input<br>• CPU_SWDIO: serial wire data<br>• ADC6: analog input channel |
| 19 | P22 | I/O | Digital/Analog | • GPIO22: general-purpose I/O<br>• CLK26M: 26 MHz clock output<br>• SD1_DATA6: data<br>• QSPI0_SCK: serial clock<br>• RGB_B4: blue data<br>• ENET_RXDV: receive data valid<br>• EXT_FLASH_SO: external flash data output<br>• ADC5: analog input channel |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 20 | P23 | I/O | Digital/Analog | • GPIO23: general-purpose I/O<br>• SD1_DATA7: data<br>• QSPI0_CS: chip select<br>• RGB_B3: blue data<br>• ENET_RXD0: receive data<br>• EXT_FLASH_SI: external flash data input<br>• ADC3: analog input channel |
| 21 | P24 | I/O | Digital/Analog | • GPIO24: general-purpose I/O<br>• LPO_CLK: 32 kHz clock output<br>• QSPI0_IO0: data<br>• RGB_G7: green data<br>• ENET_RXD1: receive data<br>• ADC2: analog input channel |
| 22 | P25 | I/O | Digital/Analog | • GPIO25: general-purpose I/O<br>• QSPI0_IO1: data<br>• RGB_G6: green data<br>• ENET_RXD2: receive data<br>• ADC1: analog input channel |
| 23 | P26 | I/O | Digital | • GPIO26: general-purpose I/O<br>• WIFI_TX_EN: Wi-Fi transmit enable<br>• QSPI0_IO2: data<br>• RGB_G5: green data<br>• ENET_RXD3: receive data |
| 24 | CSI_DP0 | - | Analog input | MIPI CSI differential input lane 0 positive |
| 25 | CSI_DN0 | - | Analog input | MIPI CSI differential input lane 0 negative |
| 26 | CSI_DP1 | - | Analog input | MIPI CSI differential input lane 1 positive |
| 27 | CSI_DN1 | - | Analog input | MIPI CSI differential input lane 1 negative |
| 28 | CSI_CP | - | Analog input | MIPI CSI differential input clock positive |
| 29 | CSI_CN | - | Analog input | MIPI CSI differential input clock negative |
| 30 | CSI_VDDH | - | Analog output | Power supply for MIPI CSI |
| 31 | CSI_REXT | - | Analog output | Reference resistor. This analog signal connects to the ground through an external resistor. |
| 32 | VDDCORE_HS | - | Analog output | High-powered digital core LDO output |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 33 | P27 | I/O | Digital | • GPIO27: general-purpose I/O<br>• FEM_LNA_EN: LNA bypass<br>• CLK_AUXS_DVP: DVP master clock, derived from CLK_320M/CLK_480M<br>• QSPI0_IO3: data<br>• DVP_MCLK: DVP master clock, derived from CLK_320M/CLK_480M |
| 34 | P28 | I/O | Digital/Analog | • GPIO28: general-purpose I/O<br>• WIFI_RX_EN: Wi-Fi receive enable<br>• CLK_AUXS: reference clock, derived from DCO/APLL/CLK_320M/CLK_480M<br>• ENET_TXEN: transmit data enable<br>• ADC4: analog input channel |
| 35 | P29 | I/O | Digital | • GPIO29: general-purpose I/O<br>• DVP_PCLK: pixel clock |
| 36 | P30 | I/O | Digital | • GPIO30: general-purpose I/O<br>• DVP_HSYNC: horizontal synchronization |
| 37 | P31 | I/O | Digital | • GPIO31: general-purpose I/O<br>• DVP_VSYNC: vertical synchronization |
| 38 | P32 | I/O | Digital | • GPIO32: general-purpose I/O<br>• DVP_PXD0: data |
| 39 | P33 | I/O | Digital | • GPIO33: general-purpose I/O<br>• DVP_PXD1: data |
| 40 | P34 | I/O | Digital | • GPIO34: general-purpose I/O<br>• DVP_PXD2: data |
| 41 | P35 | I/O | Digital | • GPIO35: general-purpose I/O<br>• DVP_PXD3: data |
| 42 | P36 | I/O | Digital | • GPIO36: general-purpose I/O<br>• DVP_PXD4: data |
| 43 | P37 | I/O | Digital | • GPIO37: general-purpose I/O<br>• DVP_PXD5: data |
| 44 | P38 | I/O | Digital | • GPIO38: general-purpose I/O<br>• DVP_PXD6: data |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 45 | P39 | I/O | Digital | • GPIO39: general-purpose I/O<br>• DVP_PXD7: data |
| 46 | P40 | I/O | Digital | • GPIO40: general-purpose I/O<br>• DVP_PXD8: data<br>• ENET_GTCLK: RGMII timing reference for TX data transfers<br>• RGB_G4: green data |
| 47 | P41 | I/O | Digital | • GPIO41: general-purpose I/O<br>• DVP_PXD9: data<br>• ENET_TXD3: transmit data<br>• RGB_G3: green data |
| 48 | P42 | I/O | Digital | • GPIO42: general-purpose I/O<br>• ENET_TXD2: transmit data<br>• RGB_G2: green data |
| 49 | P43 | I/O | Digital | • GPIO43: general-purpose I/O<br>• ENET_TXD1: transmit data<br>• RGB_R7: red data |
| 50 | P44 | I/O | Digital | • GPIO44: general-purpose I/O<br>• ENET_TXD0: transmit data<br>• RGB_R6: red data |
| 51 | P45 | I/O | Digital | • GPIO45: general-purpose I/O<br>• ENET_TXEN: transmit data enable<br>• RGB_R5: red data |
| 52 | P46 | I/O | Digital | • GPIO46: general-purpose I/O<br>• CLK_AUXS_ENET: reference clock for external Ethernet PHY, derived from DCO/APLL<br>• RGB_R4: red data |
| 53 | VDDRAM | - | Analog output | EXMEM LDO output |
| 54 | P47 | I/O | Digital | • GPIO47: general-purpose I/O<br>• ENET_MDC: management data clock<br>• RGB_R3: red data |
| 55 | P48 | I/O | Digital | • GPIO48: general-purpose I/O<br>• ENET_MDIO: management data |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • RGB_B2: blue data |
| 56 | P49 | I/O | Digital | • GPIO49: general-purpose I/O<br>• ENET_REF_CLK: RMII reference clock<br>• ENET_GRCLK: RGMII timing reference for RX data transfers<br>• RGB_B1: blue data |
| 57 | P50 | I/O | Digital | • GPIO50: general-purpose I/O<br>• ENET_RXDV: receive data valid<br>• RGB_B0: blue data |
| 58 | P51 | I/O | Digital | • GPIO51: general-purpose I/O<br>• ENET_RXD0: receive data<br>• RGB_G1: green data |
| 59 | P52 | I/O | Digital | • GPIO52: general-purpose I/O<br>• ENET_RXD1: receive data<br>• RGB_G0: green data |
| 60 | P53 | I/O | Digital | • GPIO53: general-purpose I/O<br>• ENET_RXD2: receive data<br>• RGB_R2: red data |
| 61 | P54 | I/O | Digital | • GPIO54: general-purpose I/O<br>• ENET_RXD3: receive data<br>• RGB_R1: red data |
| 62 | P55 | I/O | Digital | • GPIO55: general-purpose I/O<br>• ENET_PHY_INT: PHY interrupt input<br>• RGB_R0: red data |
| 63 | DSI_DP0 | - | Analog output | MIPI DSI differential output lane 0 positive |
| 64 | DSI_DN0 | - | Analog output | MIPI DSI differential output lane 0 negative |
| 65 | DSI_DP1 | - | Analog output | MIPI DSI differential output lane 1 positive |
| 66 | DSI_DN1 | - | Analog output | MIPI DSI differential output lane 1 negative |
| 67 | DSI_CP | - | Analog output | MIPI DSI differential output clock positive |
| 68 | DSI_CN | - | Analog output | MIPI DSI differential output clock negative |
| 69 | DSI_DP2 | - | Analog output | MIPI DSI differential output lane 2 positive |
| 70 | DSI_DN2 | - | Analog output | MIPI DSI differential output lane 2 negative |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 71 | DSI_DP3 | - | Analog output | MIPI DSI differential output lane 3 positive |
| 72 | DSI_DN3 | - | Analog output | MIPI DSI differential output lane 3 negative |
| 73 | DSI_VDDH | - | Analog output | Power supply for DSI |
| 74 | DSI_REXT | - | Analog output | Reference resistor. This analog signal connects to the ground through an external resistor. |
| 75 | VDDCORE_HS | - | Analog output | High-powered digital core LDO output |
| 76 | VDD1V8_USB | - | Analog output | 1.8 V power supply for USB |
| 77 | VDD3V3_USB | - | Analog output | 3.3 V power supply for USB |
| 78 | USB_DP | I/O | Digital | USB D+ |
| 79 | USB_DN | I/O | Digital | USB D- |
| 80 | AUDLP | - | Analog output | Audio left channel positive output |
| 81 | AUDLN | - | Analog output | Audio left channel negative output |
| 82 | AUDRN | - | Analog output | Audio right channel negative output |
| 83 | AUDRP | - | Analog output | Audio right channel positive output |
| 84 | VCCAUD | - | Analog input | Power supply for Audio |
| 85 | VCOM | - | Analog output | Audio common mode output |
| 86 | MICBIAS | - | Analog output | Microphone bias output |
| 87 | MICN1 | - | Analog input | Microphone 1 negative input |
| 88 | MICP1 | - | Analog input | Microphone 1 positive input |
| 89 | MICP2 | - | Analog input | Microphone 2 positive input |
| 90 | MICN2 | - | Analog input | Microphone 2 negative input |
| 91 | MICN3 | - | Analog input | Microphone 3 negative input |
| 92 | MICP3 | - | Analog input | Microphone 3 positive input |
| 93 | VDDDIG | - | Analog output | Digital core LDO output |
| 94 | VDDD | - | Analog output | Digital buck/LDO output |
| 95 | SWD | - | Analog output | Digital buck switch output |
| 96 | CEN | - | Analog input | Chip enable, active high |
| 97 | VDDA | - | Analog output | Analog buck/LDO output |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 98 | SWA | - | Analog output | Analog buck switch output |
| 99 | GND_DCDC | - | GND | Buck ground |
| 100 | VBAT | - | Power | Chip power supply |
| 101 | SWH | - | Analog output | High-powered digital buck switch output |
| 102 | VDDH | - | Analog output | High-powered digital buck/LDO output |
| 103 | VDDCORE_HS | - | Analog output | High-powered digital core LDO output |
| 104 | VOUT | - | Analog output | Power supply output |
| 105 | P0 | I/O | Digital/Analog | • GPIO0: general-purpose I/O<br>• CPU_SWCLK: serial wire clock<br>• ADC12: analog input channel |
| 106 | P1 | I/O | Digital/Analog | • GPIO1: general-purpose I/O<br>• CPU_SWDIO: serial wire data<br>• ADC13: analog input channel |
| 107 | P2 | I/O | Digital | • GPIO2: general-purpose I/O<br>• SD0_CLK: clock<br>• QSPI1_SCK: serial clock |
| 108 | P3 | I/O | Digital | • GPIO3: general-purpose I/O<br>• SD0_CMD: command/response<br>• QSPI1_CS: chip select |
| 109 | P4 | I/O | Digital | • GPIO4: general-purpose I/O<br>• SD0_DATA0: data<br>• QSPI1_IO0: data |
| 110 | P5 | I/O | Digital | • GPIO5: general-purpose I/O<br>• SD0_DATA1: data<br>• QSPI1_IO1: data |
| 111 | P6 | I/O | Digital | • GPIO6: general-purpose I/O<br>• CLK13M: 26 MHz clock output (divide by 1/2/3/4)<br>• SD0_DATA4: data<br>• QSPI1_IO2: data |
| 112 | P7 | I/O | Digital | • GPIO7: general-purpose I/O<br>• SD0_DATA5: data |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| | | | | • QSPI1_IO3: data |
| 113 | P8 | I/O | Digital/Analog | • GPIO8: general-purpose I/O<br>• SD0_DATA6: data<br>• ADC10: analog input channel<br>• 32K_XO: 32.768 kHz crystal output |
| 114 | P9 | I/O | Digital/Analog | • GPIO9: general-purpose I/O<br>• SD0_DATA7: data<br>• 32K_XI: 32.768 kHz crystal input |
| 115 | P10 | I/O | Digital | • GPIO10: general-purpose I/O<br>• DL_UART_RX: UART flash download receive data input (UART0)<br>• SD0_DATA2: data<br>• CLK_AUXS: reference clock, derived from DCO/APLL/CLK_320M/CLK_480M |
| 116 | P11 | I/O | Digital | • GPIO11: general-purpose I/O<br>• DL_UART_TX: UART flash download transmit data output (UART0)<br>• SD0_DATA3: data |
| 117 | VDDDIG | - | Analog output | Digital core LDO output |
| 118 | P12 | I/O | Digital/Analog | • GPIO12: general-purpose I/O<br>• ADC14: analog input channel |
| 119 | P13 | I/O | Digital/Analog | • GPIO13: general-purpose I/O<br>• ENET_GTCLK: RGMII timing reference for TX data transfers<br>• ADC15: analog input channel |
| 120 | VDDGPIO | - | Analog output | Power supply for GPIOs |
| 121 | P56 | I/O | Digital | GPIO56: general-purpose I/O |
| 122 | P57 | I/O | Digital | GPIO57: general-purpose I/O |
| 123 | P58 | I/O | Digital | GPIO58: general-purpose I/O |
| 124 | P59 | I/O | Digital | • GPIO59: general-purpose I/O<br>• CLK_AUXS_DVP: DVP master clock, derived from CLK_320M/CLK_480M |
| 125 | P60 | I/O | Digital | • GPIO60: general-purpose I/O<br>• ENET_PHY_INT: PHY interrupt input |

| Pin # | Name | I/O | Type | Description |
|---|---|---|---|---|
| 126 | P61 | I/O | Digital | GPIO61: general-purpose I/O |
| 127 | P62 | I/O | Digital | • GPIO62: general-purpose I/O<br>• UART4_RX: receive data input |
| 128 | P63 | I/O | Digital | • GPIO63: general-purpose I/O<br>• UART4_TX: transmit data output |
| Die pad | GND_SLUG | - | GND | Ground |

## 3.2 Pin Multiplexing

High-performance peripherals have alternate functions mapped onto fixed I/O pins. For normal peripherals, through the I/O multiplexer (I/O MUX), their input signals can be from any I/O pin, and their output signals can be routed to any I/O pin. Functions of 64 GPIOs are selected through registers GPIO_FUNC_CFG0 to GPIO_FUNC_CFG15. Each GPIO_FUNC_CFG register controls four GPIOs.

Table 3-2 shows the pin multiplexing of high-performance peripherals.

**Table 3-2 Pin Multiplexing of High-performance Peripherals**

| GPIO | Flash Download | Alternate Functions (Configured Through Registers GPIO_FUNC_CFG0–15) | | | | | | | | Analog Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AF1 (8'd126) | AF2 (8'd129) | AF3 (8'd130) | AF4 (8'd131) | AF5 (8'd132) | AF6 (8'd133) | AF7 (8'd134) | AF8 (8'd135) | Analog1 | Analog2 |
| | UART | Clock/<br>AoA/AoD<br>FEM Support | CPU SWD<br>SDMMC0/1<br>DVP<br>Clock | QSPI0/1<br>Clock<br>ENET | DISPLAY<br>DVP | ENET | External Flash | CPU SWD | GPIO | XTALL | AUX ADC |
| GPIO0 | | | CPU_SWCLK | | | | | | GPIO | | ADC12 |
| GPIO1 | | | CPU_SWDIO | | | | | | GPIO | | ADC13 |
| GPIO2 | | | SD0_CLK | QSPI1_SCK | | | | | GPIO | | |
| GPIO3 | | | SD0_CMD | QSPI1_CS | | | | | GPIO | | |
| GPIO4 | | | SD0_DATA0 | QSPI1_IO0 | | | | | GPIO | | |
| GPIO5 | | | SD0_DATA1 | QSPI1_IO1 | | | | | GPIO | | |
| GPIO6 | | CLK13M | SD0_DATA4 | QSPI1_IO2 | | | | | GPIO | | |
| GPIO7 | | | SD0_DATA5 | QSPI1_IO3 | | | | | GPIO | | |
| GPIO8 | | | SD0_DATA6 | | | | | | GPIO | 32K_XO | ADC10 |

| GPIO | Flash Download | Alternate Functions (Configured Through Registers GPIO_FUNC_CFG0–15) | | | | | | | | Analog Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AF1 (8'd126) | AF2 (8'd129) | AF3 (8'd130) | AF4 (8'd131) | AF5 (8'd132) | AF6 (8'd133) | AF7 (8'd134) | AF8 (8'd135) | Analog1 | Analog2 |
| | UART | Clock/<br>AoA/AoD<br>FEM Support | CPU SWD<br>SDMMC0/1<br>DVP<br>Clock | QSPI0/1<br>Clock<br>ENET | DISPLAY<br>DVP | ENET | External Flash | CPU SWD | GPIO | XTALL | AUX ADC |
| GPIO9 | | | SD0_DATA7 | | | | | | GPIO | 32K_XI | |
| GPIO10 | DL_UART_RX | | SD0_DATA2 | CLK_AUXS | | | | | GPIO | | |
| GPIO11 | DL_UART_TX | | SD0_DATA3 | | | | | | GPIO | | |
| GPIO12 | | | | | | | | | GPIO | | ADC14 |
| GPIO13 | | | | | | ENET_GTCLK | | | GPIO | | ADC15 |
| GPIO14 | | BT_ANT0 | SD1_CLK | | RGB_DE | ENET_TXD3 | | | GPIO | | |
| GPIO15 | | BT_ANT1 | SD1_CMD | | RGB_VSYNC | ENET_TXD2 | | | GPIO | | |
| GPIO16 | | BT_ANT2 | SD1_DATA0 | | RGB_HSYNC | ENET_TXD1 | | | GPIO | | |
| GPIO17 | | BT_ANT3 | SD1_DATA1 | | RGB_DISP | ENET_TXD0 | | | GPIO | | |
| GPIO18 | | | SD1_DATA2 | | RGB_DCLK | CLK_AUXS_ENET | | | GPIO | | |
| GPIO19 | | | SD1_DATA3 | | RGB_B7 | ENET_MDC | | | GPIO | | |
| GPIO20 | | | SD1_DATA4 | | RGB_B6 | ENET_MDIO | EXT_FLASH_CSN | CPU_SWCLK | GPIO | | |
| GPIO21 | | | SD1_DATA5 | ENET_REF_CLK | RGB_B5 | ENET_GRCLK | EXT_FLASH_SCK | CPU_SWDIO | GPIO | | ADC6 |
| GPIO22 | | CLK26M | SD1_DATA6 | QSPI0_SCK | RGB_B4 | ENET_RXDV | EXT_FLASH_SO | | GPIO | | ADC5 |
| GPIO23 | | | SD1_DATA7 | QSPI0_CS | RGB_B3 | ENET_RXD0 | EXT_FLASH_SI | | GPIO | | ADC3 |
| GPIO24 | | LPO_CLK | | QSPI0_IO0 | RGB_G7 | ENET_RXD1 | | | GPIO | | ADC2 |

| GPIO | Flash Download | Alternate Functions (Configured Through Registers GPIO_FUNC_CFG0–15) | | | | | | | | Analog Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AF1 (8'd126) | AF2 (8'd129) | AF3 (8'd130) | AF4 (8'd131) | AF5 (8'd132) | AF6 (8'd133) | AF7 (8'd134) | AF8 (8'd135) | Analog1 | Analog2 |
| | UART | Clock/<br>AoA/AoD<br>FEM Support | CPU SWD<br>SDMMC0/1<br>DVP<br>Clock | QSPI0/1<br>Clock<br>ENET | DISPLAY<br>DVP | ENET | External Flash | CPU SWD | GPIO | XTALL | AUX ADC |
| GPIO25 | | | | QSPI0_IO1 | RGB_G6 | ENET_RXD2 | | | GPIO | | ADC1 |
| GPIO26 | | WIFI_TX_EN | | QSPI0_IO2 | RGB_G5 | ENET_RXD3 | | | GPIO | | |
| GPIO27 | | FEM_LNA_EN | CLK_AUXS_DVP | QSPI0_IO3 | DVP_MCLK | | | | GPIO | | |
| GPIO28 | | WIFI_RX_EN | CLK_AUXS | | | ENET_TXEN | | | GPIO | | ADC4 |
| GPIO29 | | | DVP_PCLK | | | | | | GPIO | | |
| GPIO30 | | | DVP_HSYNC | | | | | | GPIO | | |
| GPIO31 | | | DVP_VSYNC | | | | | | GPIO | | |
| GPIO32 | | | DVP_PXD0 | | | | | | GPIO | | |
| GPIO33 | | | DVP_PXD1 | | | | | | GPIO | | |
| GPIO34 | | | DVP_PXD2 | | | | | | GPIO | | |
| GPIO35 | | | DVP_PXD3 | | | | | | GPIO | | |
| GPIO36 | | | DVP_PXD4 | | | | | | GPIO | | |
| GPIO37 | | | DVP_PXD5 | | | | | | GPIO | | |
| GPIO38 | | | DVP_PXD6 | | | | | | GPIO | | |
| GPIO39 | | | DVP_PXD7 | | | | | | GPIO | | |
| GPIO40 | | | DVP_PXD8 | ENET_GTCLK | RGB_G4 | | | | GPIO | | |

| GPIO | Flash Download | Alternate Functions (Configured Through Registers GPIO_FUNC_CFG0–15) | | | | | | | | Analog Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AF1 (8'd126) | AF2 (8'd129) | AF3 (8'd130) | AF4 (8'd131) | AF5 (8'd132) | AF6 (8'd133) | AF7 (8'd134) | AF8 (8'd135) | Analog1 | Analog2 |
| | UART | Clock/<br>AoA/AoD<br>FEM Support | CPU SWD<br>SDMMC0/1<br>DVP<br>Clock | QSPI0/1<br>Clock<br>ENET | DISPLAY<br>DVP | ENET | External Flash | CPU SWD | GPIO | XTALL | AUX ADC |
| GPIO41 | | | DVP_PXD9 | ENET_TXD3 | RGB_G3 | | | | GPIO | | |
| GPIO42 | | | | ENET_TXD2 | RGB_G2 | | | | GPIO | | |
| GPIO43 | | | | ENET_TXD1 | RGB_R7 | | | | GPIO | | |
| GPIO44 | | | | ENET_TXD0 | RGB_R6 | | | | GPIO | | |
| GPIO45 | | | | ENET_TXEN | RGB_R5 | | | | GPIO | | |
| GPIO46 | | | | CLK_AUXS_ENET | RGB_R4 | | | | GPIO | | |
| GPIO47 | | | | ENET_MDC | RGB_R3 | | | | GPIO | | |
| GPIO48 | | | | ENET_MDIO | RGB_B2 | | | | GPIO | | |
| GPIO49 | | | ENET_REF_CLK | ENET_GRCLK | RGB_B1 | | | | GPIO | | |
| GPIO50 | | | | ENET_RXDV | RGB_B0 | | | | GPIO | | |
| GPIO51 | | | | ENET_RXD0 | RGB_G1 | | | | GPIO | | |
| GPIO52 | | | | ENET_RXD1 | RGB_G0 | | | | GPIO | | |
| GPIO53 | | | | ENET_RXD2 | RGB_R2 | | | | GPIO | | |
| GPIO54 | | | | ENET_RXD3 | RGB_R1 | | | | GPIO | | |
| GPIO55 | | | | ENET_PHY_INT | RGB_R0 | | | | GPIO | | |
| GPIO56 | | | | | | | | | GPIO | | |

| GPIO | Flash Download | Alternate Functions (Configured Through Registers GPIO_FUNC_CFG0–15) | | | | | | | | Analog Functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | AF1 (8'd126) | AF2 (8'd129) | AF3 (8'd130) | AF4 (8'd131) | AF5 (8'd132) | AF6 (8'd133) | AF7 (8'd134) | AF8 (8'd135) | Analog1 | Analog2 |
| | UART | Clock/<br>AoA/AoD<br>FEM Support | CPU SWD<br>SDMMC0/1<br>DVP<br>Clock | QSPI0/1<br>Clock<br>ENET | DISPLAY<br>DVP | ENET | External Flash | CPU SWD | GPIO | XTALL | AUX ADC |
| GPIO57 | | | | | | | | | GPIO | | |
| GPIO58 | | | | | | | | | GPIO | | |
| GPIO59 | | | CLK_AUXS_DVP | | | | | | GPIO | | |
| GPIO60 | | | | ENET_PHY_INT | | | | | GPIO | | |
| GPIO61 | | | | | | | | | GPIO | | |
| GPIO62 | | | UART4_RX | | | | | | GPIO | | |
| GPIO63 | | | UART4_TX | | | | | | GPIO | | |

**Table 3-3 GPIO Matrix of Normal Peripherals**

| Peripheral | GPIO_FUNC_CFGx Value | GPIO Function | Description |
|---|---|---|---|
| GPIO | 8'd0 | GPIO | General-purpose I/O |
| SPI0 | 8'd1 | SPI0_MISO | Master in slave out |
| | 8'd2 | SPI0_MOSI | Master out slave in |
| | 8'd3 | SPI0_CSN | Chip select |
| | 8'd4 | SPI0_SCK | Serial clock |
| SPI1 | 8'd5 | SPI1_MISO | Master in slave out |
| | 8'd6 | SPI1_MOSI | Master out slave in |
| | 8'd7 | SPI1_CSN | Chip select |
| | 8'd8 | SPI1_SCK | Serial clock |
| SPI2 | 8'd9 | SPI2_MISO | Master in slave out |
| | 8'd10 | SPI2_MOSI | Master out slave in |
| | 8'd11 | SPI2_CSN | Chip select |
| | 8'd12 | SPI2_SCK | Serial clock |
| I3C | 8'd13 | I3C_SCL | Serial clock |
| | 8'd14 | I3C_SDA | Serial data |
| | 8'd15 | I3C_SDA_PURN | Serial data pull-up enable, active low |
| CAN | 8'd17 | CAN_RX | Receive |
| | 8'd18 | CAN_STBY | Transceiver standby mode, active high |
| | 8'd19 | CAN_TX | Transmit |
| DMIC1 | 8'd23 | DMIC1_CLK | Clock |
| | 8'd24 | DMIC1_DAT | Data |
| DMIC0 | 8'd27 | DMIC0_CLK | Clock |
| | 8'd28 | DMIC0_DAT | Data |
| HDMI CEC | 8'd29 | HDMI_CEC | Data |
| I2C0 | 8'd30 | I2C0_SCL | Serial clock |
| | 8'd31 | I2C0_SDA | Serial data |

| Peripheral | GPIO_FUNC_CFGx Value | GPIO Function | Description |
|---|---|---|---|
| I2C1 | 8'd32 | I2C1_SCL | Serial clock |
| | 8'd33 | I2C1_SDA | Serial data |
| I2C2 | 8'd34 | I2C2_SCL | Serial clock |
| | 8'd35 | I2C2_SDA | Serial data |
| I2C3 | 8'd36 | I2C3_SCL | Serial clock |
| | 8'd37 | I2C3_SDA | Serial data |
| I2S0 | 8'd38 | I2S0_DIN | Serial data input |
| | 8'd39 | I2S0_DOUT | Serial data output |
| | 8'd40 | I2S0_SCK | Serial clock |
| | 8'd41 | I2S0_SYNC | Frame synchronization |
| I2S1 | 8'd42 | I2S1_DIN | Serial data input |
| | 8'd43 | I2S1_DOUT | Serial data output |
| | 8'd44 | I2S1_SCK | Serial clock |
| | 8'd45 | I2S1_SYNC | Frame synchronization |
| I2S2 | 8'd46 | I2S2_DIN | Serial data input |
| | 8'd47 | I2S2_DOUT | Serial data output |
| | 8'd48 | I2S2_SCK | Serial clock |
| | 8'd49 | I2S2_SYNC | Frame synchronization |
| I2S3 | 8'd50 | I2S3_DIN | Serial data input |
| | 8'd51 | I2S3_DOUT | Serial data output |
| | 8'd52 | I2S3_SCK | Serial clock |
| | 8'd53 | I2S3_SYNC | Frame synchronization |
| I2S | 8'd54 | I2S_MCLK | Master clock |
| IRDA | 8'd55 | IRDA | Data |
| SWD | 8'd57 | SWCLK | Serial wire clock |
| | 8'd58 | SWDIO | Serial wire data |
| LIN | 8'd59 | LIN_RXD | Receive data input |
| | 8'd60 | LIN_SLEEP | Transceiver sleep mode, active low |

| Peripheral | GPIO_FUNC_CFGx Value | GPIO Function | Description |
|---|---|---|---|
| | 8'd61 | LIN_TXD | Transmit data output |
| PWM | 8'd65 | PWM0 | PWM0 |
| | 8'd66 | PWM1 | PWM1 |
| | 8'd67 | PWM2 | PWM2 |
| | 8'd68 | PWM3 | PWM3 |
| | 8'd69 | PWM4 | PWM4 |
| | 8'd70 | PWM5 | PWM5 |
| | 8'd71 | PWM6 | PWM6 |
| | 8'd72 | PWM7 | PWM7 |
| | 8'd73 | PWM8 | PWM8 |
| | 8'd74 | PWM9 | PWM9 |
| | 8'd75 | PWM10 | PWM10 |
| | 8'd76 | PWM11 | PWM11 |
| SC | 8'd77 | SC_CLK | Clock |
| | 8'd78 | SC_IO | Data input/output |
| | 8'd79 | SC_RSTN | Reset |
| | 8'd80 | SC_VCC | Power supply to the smart card |
| SPDIF0 | 8'd85 | SPDIF0_RX | Receive |
| | 8'd86 | SPDIF0_TX | Transmit |
| SPDIF1 | 8'd87 | SPDIF1_RX | Receive |
| | 8'd88 | SPDIF1_TX | Transmit |
| UART0 | 8'd89 | UART0_CTS | Clear to send |
| | 8'd90 | UART0_RTS | Request to send |
| | 8'd91 | UART0_RX | Receive data input |
| | 8'd92 | UART0_TX | Transmit data output |
| UART1 | 8'd93 | UART1_RX | Receive data input |
| | 8'd94 | UART1_TX | Transmit data output |
| UART2 | 8'd95 | UART2_RX | Receive data input |

| Peripheral | GPIO_FUNC_CFGx Value | GPIO Function | Description |
|---|---|---|---|
| | 8'd96 | UART2_TX | Transmit data output |
| UART3 | 8'd97 | UART3_RX | Receive data input |
| | 8'd98 | UART3_TX | Transmit data output |

# 4. Functional Description

## 4.1 Wi-Fi/Bluetooth Transceiver

The BK7259 integrates a high-performance Wi-Fi/Bluetooth transceiver. The transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with only one ANT pin connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

## 4.2 FEM Support

The BK7259 supports the use of an external Front-End Module (FEM). The external FEMs are controlled by three signals WIFI_TX_EN, WIFI_RX_EN, and FEM_LNA_EN.

**Table 4-1 FEM Operating Modes**

| Operating Mode | WIFI_TX_EN (GPIO26) | WIFI_RX_EN (GPIO28) | FEM_LNA_EN (GPIO27) |
|---|---|---|---|
| Transmit mode | 1 | 0 | 0 |
| Receive mode | 0 | 1 | 1 |
| LNA bypass mode | 0 | 1 | 0 |
| | 1 | 1 | X |
| Standby mode | 0 | 0 | 0 |
| Not supported | All other states | | |

## 4.3 Clock Management

The primary clock sources available in the BK7259 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator: it outputs clock signal XTALH
  - 160–640 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO

- 960 MHz digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M

- Low-frequency clocks
  - 32 kHz (32.768 kHz) crystal oscillator: it outputs clock signal XTALL
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Audio clock
  - 90–99 MHz audio PLL (APLL): it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL
- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC

The BK7259 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK13M: clock derived from CLK_XTAL (factor 1/2/3/4)
- CLK26M: high-frequency crystal clock CLK_XTAL, generally 26 MHz
- LPO_CLK: LPO_CLK clock
- I2S_MCLK: reference clock for external audio codec, derived from APLL
- CLK_AUXS: reference clock, derived from DCO/APLL/CLK_320M/CLK_480M (factor 1 to16)
- CLK_AUXS_ENET: reference clock for external Ethernet PHY, derived from DCO/APLL (factor 1 to 16)
- DVP_MCLK: reference clock for external DVP sensor, derived from CLK_320M/CLK_480M (factor 1 to 16)
- CLK_AUXS_DVP: reference clock for external DVP sensor, derived from CLK_320M/CLK_480M (factor 1 to 16)

## 4.4 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset, brown-out reset, and AWDT watchdog reset reset the whole chip to its initial state. The CPU core reset resets each respective CPU core.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

## 4.5 Power Modes

The BK7259 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

**Shutdown Mode:** All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

**Deep Sleep Mode:** All circuits are powered down except the AON block. GPIOs or RTC can power up the system again. The retention register holds its content.

**Sleep Mode:** The MCU and all digital blocks stop their clocks. GPIOs, RTC, or Wi-Fi/Bluetooth MAC low-power counters can bring the system back to active mode with normal voltage.

**Active Mode:** The MCU is active, and all peripherals are available.

## 4.6 General-purpose I/Os (GPIO)

The BK7259 has up to 64 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions and/or analog functions. Section 3.2 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Analog function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

## 4.7 SPI Interfaces (SPI)

The BK7259 integrates three SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 40 MHz in both master and slave modes.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width

- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

## 4.8 Quad SPI Interfaces (QSPI)

The BK7259 embeds two Quad SPI interfaces that provide support for communicating with external flash, PSRAM, or AMOLED display. The QSPI interfaces allow communicating up to 80 MHz.

The features of the QSPI interfaces are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

## 4.9 UART Interfaces (UART)

The BK7259 includes five Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 5 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0)
- Flash download (UART0)
- CPU core debugging (UART4)
- Programmable digital filter

## 4.10 Smart Card Controller (SC)

The BK7259 features a Smart Card controller (SC). The Smart Card controller is a communication controller that transmits data between the superior system and the Smart Card. It can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

The features of the Smart Card controller (SC) are listed below:

- Supports the ISO/IEC 7816-3:2006 and EMV 4.3 specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Adjustable FIFOs for Receive and Transmit buffers (64 bytes) with threshold
- Configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers

## 4.11 SD and eMMC Host Controllers (SDMMC)

Two SD/SDIO and eMMC host controllers (SDMMC) are available on the BK7259. The SDMMC can be used as a host to communicate with external SD cards, SDIO cards, and eMMC devices.

The features of the SDMMC include the following:

- Embedded MultiMediaCard System Specification version 5.1 compliant

- Card support for three data bus modes: 1-bit (default), 4-bit, and 8-bit

- SD memory card specifications version 4.20 compliant
  - SPI mode and UHS-II mode not supported
- SDIO card specification version 4.10 compliant
  - Card support for two data bus modes: 1-bit (default) and 4-bit
  - SPI mode and UHS-II mode not supported
- Supports SDMA/ADMA2/ADMA3 transfers, allowing high-speed transfer without CPU load
- Data and command output enable signals allow control of external bidirectional drivers
- Supports Command Queuing Engine (CQE) and compliant with eMMC CQ HCI
  - Programmable scheduler algorithm selection of task execution
  - Supports data prefetch for back-to-back WRITE operations
- Supports fully software driven tuning operations

## 4.12 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7259 embeds four I2C interfaces, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

## 4.13 I3C Interface (I3C)

Improved Inter-Integrated Circuit (I3C) is a two-wire, shared (multidrop), serial communication interface developed by the MIPI Alliance to enhance the legacy I2C interface. The BK7259 includes an I3C interface.

The I3C interface supports the following key features:

- I3C transmission modes:
  - Single data rate messaging (SDR):
    - Fm/Fm+

- 11 MHz to 12.9 MHz (mixed fast bus)
- Up to 12.9 MHz (pure bus)

- High data rate messaging (HDR):
  - HDR-DDR

- Dynamic address assignment
- I3C slave generated requests:
  - In-band interrupt
  - Hot-join request
  - Mastership request
- I3C common command codes
- Time control:
  - Asynchronous Mode 0
- Legacy I2C device co-existence on the same bus
- Retaining registers
- Command queue
- Immediate commands
- Separate TX, RX, and IBI storage elements
- MCTP flow control
- General-purpose inputs/outputs accessible tough I3C I/F
- Multi-role (main master, secondary master, slave)
- Target reset
- Group addressing

## 4.14 USB Controller (USB)

The BK7259 embeds a USB high-speed (up to 480 Mbps) controller with an integrated transceiver. It can operate as a host or a device.

The USB controller features are the following:

- Compliant with the Universal Serial Bus Specification Rev 1.1 and 2.0
- Full-speed (FS) operation (up to 12 Mbps) and high-speed operation (up to 480 Mbps)
- One bidirectional control endpoint0
- Seven IN/OUT endpoints configurable to support bulk, interrupt or isochronous data transfer

- A FIFO of 8 Kbytes configurable to be allocated to 8 endpoints
- USB 2.0 Link Power Management (LPM) support

## 4.15 CAN Controller (CAN)

The BK7259 features a Controller Area Network (CAN) controller. The CAN controller uses the basic CAN principle and meets all constraints of the CAN-specification 2.0B active. Furthermore, the CAN controller can be configured to meet the specification of CAN with flexible data rate CAN FD. CAN 2.0 carries a data payload up to 8 bytes and CAN FD up to 64 bytes.

The CAN controller supports two operating modes, normal and standby, which can be selected via the CAN_STBY pin. If a high level is applied to the CAN_STBY pin, the external transceiver enters the standby mode.

## 4.16 LIN Controller (LIN)

The BK7259 has a Local Interconnect Network (LIN) controller. The LIN controller is a communication controller that performs serial communication. It implements the data link layer of the LIN Protocol Specification. The LIN protocol uses a single master/multiple slave concept for the frame transfer between nodes of the LIN network.

The LIN controller supports Sleep mode. If a low level is applied to the LIN_SLEEP pin, the external transceiver enters the Sleep mode.

The features of the LIN controller are listed here:

- Support of LIN specification 2.2A
- Backward compatibility to LIN 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 kbit/s and 20 kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface

## 4.17 GDMA Controller (GDMA)

The BK7259 has a general-purpose DMA controller (GDMA) with 8 DMA channels to unload CPU activity. The 8 channels are shared by peripherals that have GDMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controllers allow peripheral to memory, memory to memory, and memory to peripheral, peripheral to peripheral data transfers at a high speed.

The GDMA controller supports channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of peripherals on the BK7259 have GDMA capabilities, including UART0, UART1, UART2, UART3, SPI0, SPI1, SPI2, I2S0, I2S1, I2S2, I2S3, AUDIO, and AUX ADC.

## 4.18 High-performance DMA Controller (HPDMA)

The BK7259 has a high-performance DMA controller (HPDMA) with 8 DMA channels to offload CPU activity. The HPDMA controller performs programmable data transfers between memory-mapped peripherals and/or memories via linked-lists.

The HPDMA controller has the features below:

- Dual bidirectional AXI master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
- Programmable data width for destination and source:
  - 8 bits (byte)
  - 16 bits (half-word)
  - 32 bits (word)
  - 64 bits
  - 128 bits
- Eight-grade priority for transfers arbitration at a channel level

- Per channel event generation on the following events: transfer complete, half transfer complete, internal FIFO error, and bus error
- Each channel can be independently configured to generate interrupts for specific events.
- 8 concurrent DMA channels:
  - Each channel has a FIFO for queuing source and destination transfers.
  - Intra-channel DMA transfers chaining using programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Number of data bytes to be transferred from the source can be programmed for each block.
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Event generation on DMA half-transfer complete and transfer complete
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Support for channel suspend and resume
  - Channel status reporting, including FIFO level and event flags
- Secure/non-secure support:
  - Support for secure and non-secure DMA transfers, independently at a channel level
  - TrustZone-aware AXI master port
  - TrustZone-aware AHB slave port
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AXI master port
  - Privileged-aware AHB slave port

UART4 on the BK7259 can utilize these HPDMA channels.

## 4.19 Ethernet MAC Interface (ENET)

The BK7259 provides a media access controller (MAC) for Ethernet LAN communications through a reduced medium-independent interface (RMII) or a reduced gigabit media independent interface (RGMII). The Ethernet MAC interface (ENET) is compliant with the IEEE 802.3-2015 specification and can be used in applications such as network

interface cards, and data center bridges and nodes. The BK7259 requires an external physical interface device (PHY) to connect to the physical LAN bus. The PHY is connected to the device RMII port using 9 signals or RGMII port using 14 signals, and can be clocked using a 25 MHz clock from the BK7259 or an external crystal oscillator.

The ENET includes the following features:

- 10, 100, and 1000 Mbps data transfer rates
- Half-duplex (CSMA/CD) and full-duplex operation
- 32-bit CRC generation and removal
- Tagged MAC frame support (VLAN support)
- Dedicated DMA controller allowing high-speed transfers between the system memory and the internal FIFOs
- Embedded TX FIFO and RX FIFO to buffer transmit and receive frames. Both FIFOs are 2 Kbytes.
- MAC control sublayer (control frames) support
- Different types of address filtering for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588-2008 (version 2)
- Triggers interrupt when system time becomes greater than target time

## 4.20 PWM

The BK7259 has an advanced-control PWM module (PWM). The PWM module consists of 12 32-bit auto-reload counters driven by 12 programmable prescalers. The PWM module has 12 independent channels for input capture, pulse edge counting, or generation of output waveforms (output compare).

The 12 independent channels can be allocated to any counter/comparator output. Each of the 12 channels can generate independent waveforms or complementary waveforms when coupled with any other channels.

The features of the PWMG are listed here:

- 12 32-bit up, down, or up-and-down auto-reload counters
- 12 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- 12 independent channels for:
  - Input capture
  - Pulse edge counting
  - PWM generation (edge or center-aligned mode)
- Complementary outputs with programmable dead-time and configurable dead-time mode

- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

# 4.21 Video Peripherals

## 4.21.1 Display Controller (DISPLAY)

The TFT LCD display controller (DISPLAY) provides a 24-bit parallel digital RGB (Red, Green, Blue) and outputs all signals to interfaces of various LCD and TFT panels.

The display controller has the following features:

- Up to 24-bit RGB parallel pixel output
- Input from the GPU, input color format: tiled HV sampled ARGB8888 1 bpp
- Three output color formats:
  - RBG888
  - RBG666
  - RBG565
- Programmable clocks for different display panels
- Configurable window position and size
- AXI master interface with burst of 64 words

## 4.21.2 Display Serial Interface (DSI)

The display serial interface (DSI) provides an interface for communicating with MIPI DSI compliant displays. It supports for up to four D-PHY data lanes, data rate up to 1.5 Gbps per lane.

### 4.21.3 Digital Video Port Interface (DVP)

The digital video port (DVP) interface provides a 10-bit parallel interface to sensors. The input from the sensor is fed to the video processors, and the output of the video processors is written to the data memory.

The DVP interface features include:

- 10-bit parallel interface
- Programmable polarity for pixel clock and synchronization signals

### 4.21.4 Camera Serial Interface (CSI)

The camera serial interface (CSI) provides an interface for communicating with MIPI CSI compliant cameras. It supports for up to two D-PHY data lanes, data rate up to 1.5 Gbps per lane.

### 4.21.5 Image Signal Processor (ISP)

The image signal processor (ISP) provides a wide range of image processing features with less power consumption. It offers image processing features with support for DVP/MIPI CSI sensors and DMA data.

The ISP provides the following features:

- Input format: RAW (8-, 10-, 12-bit)/YUV (BT.601/656)
- Resolution: maximum to 2560*2560
- Functional feature
  - Test pattern generator (TPG)
  - Black level subtraction (BLS)
  - Gamma-in/out
  - Lens shade correction (LSC)
  - Digital gain
  - Wide dynamic range (WDR) tone mapping
  - Green equalization (GE)
  - Defect pixel correction (DPC)
  - NR (noise reduction)
  - Demosaic interpolation
  - Color correction (CC)
  - Color adjustment (hue, brightness, contrast, saturation)

- 3A (AE/AWB/AF)
- Anti-flicker
- Color aberration correction (CAC)

- Output: 2 paths (YUV420/422, RGB888, RAW8-12)
- Post-processor: crop, arbitrary factor downscale

### 4.21.6 Video Processing Unit (VPU)

The video processing unit (VPU) is designed specifically for video codecs and video processing. It includes a hardware video pre-processor, a hardware video decoder, a hardware video encoder, and a hardware video post-processor.

The VPU offers the following features:

- Pre-processor
  - YUV422/RGB to YUV420
  - Crop (maximum 32768*32768)
  - OSD (8 rectangle drawing, YUV/RGB)
  - Mosaic
- Encoder
  - Maximum resolution: 2560*2560
  - H.264 (BP/MP/HP), 2 paths
  - JPEG (JFIF/MJPEG)
  - ROI (Region of Interest)
  - CBR/VBR/ABR/CVBR/CQP
  - Input format: YUV420/422, RGB888/565/444/101010
- Decoder
  - Maximum resolution: 1920*1080
  - H.264 (BP/MP/HP), YUV420 output
  - JPEG: YUV400/420/422/444
- Post-processor
  - Up/down scaling (up to 3x/down)
  - YUV to RGB

## 4.21.7 Graphics Processing Unit (GPU)

The graphics processing unit (GPU) provides hardware acceleration for graphics processing, to bring high-end graphic capabilities to a variety of IoT devices.

The GPU supports the following features:

- Input format
  - ARGB2222/1555/4444/8565/8888
  - RGB565/888
  - YUY2/NV12
- Tessellation: Lines, quadratics and cubic Bezier curves
- Vector Graphics
  - Compression: visual lossless from 1.6 to 3.0
  - Blending: 8 porter duff modes
  - Any angle rotation
  - Linear and curved paint paths
  - Filter and interpolation

## 4.21.8 Display Processor Unit (DPU)

The display processor unit (DPU) outputs video and graphic streams from a single output panel with up to 1080p display resolution. The single output panel can connect to a Display Pixel Interface (DPI), enhanced Display Pixel Interface (eDPI), or Display Bus Interface (DBI) device for RGB output or a QSPI device for RGB and monochrome output.

The features of the DPU are as follows:

- Input format
  - RGB888/565 (linear and tiled)
  - ARGB8565/8888 (linear and tiled)
  - YUY2/NV12
- Pre-processor
  - Rotation (90, 180, 270)/flip
  - YUV to RGB
  - Color keying
  - Cursor: 32*32 ARGB
- Post-processor

- Alpha blending (3 layers + cursor)
- Gamma
- Dithering
- RCD (round corner display) blending

- Output interface
  - MIPI DSI (DPI/DBI/eSPI), QSPI, and RGB
  - Maximum 1920*1080 for linear output
  - Maximum 1024*768 for tiled output

# 4.22 Audio Peripherals

The BK7259 comes with a rich set of audio peripherals to enhance the listening experience.

## 4.22.1 20-band Digital Equalizer (EQ)

A dedicated 20-band digital equalizer is implemented prior to digital-to-analog conversion, allowing the user to customize the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

## 4.22.2 Audio ADCs and DACs

The BK7259 contains three 24-bit ADCs with a sampling rate of 8 kHz, 12 kHz, 16 kHz, 24 kHz, 32 kHz, or 48 kHz. The chip also integrates two 24-bit DACs with a sampling rate of 8 kHz, 16 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, or 96 kHz.

## 4.22.3 Microphone Input Amplifiers and Bias Generator

The BK7259 contains three fully differential analog microphone input amplifiers and a low-noise microphone bias generator, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with the amplifier over a 0 to 32 dB gain range with a 2 dB step size.

## 4.22.4 Audio Amplifiers

The BK7259 provides two audio amplifiers capable of driving two 16 Ω speakers with load capacitance up to 30 pF.

### 4.22.5 Digital Microphone Interfaces (DMIC)

The BK7259 has two digital microphone interfaces. Each DMIC interface supports up to two digital microphones. The DMIC interface captures PDM stream from digital microphones and converts it to PCM data. The PCM sampling rate can be up to 384 kHz when the PDM clock frequency is 3.072 MHz.

### 4.22.6 SPDIF Interfaces (SPDIF)

The BK7259 integrates two SPDIF Interfaces. The SPDIF interface is a digital audio interface used to carry uncompressed PCM audio or compressed surround sound.

### 4.22.7 HDMI CEC Controller (HDMI CEC)

The BK7259 provides a high-definition multimedia interface (HDMI) consumer electronics control (CEC) controller. The HDMI CEC controller is designed to control HDMI connected audiovisual devices in an environment.

### 4.22.8 I2S Interfaces (I2S)

The BK7259 integrates four I2S interfaces that support master and slave modes with a sampling rate from 8 kHz to 384 kHz. The I2S interfaces support both PCM mono channel mode and I2S stereo channel mode.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels

- Master clock can be output to drive external audio devices.

## 4.23 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 54 kHz to 1.625 MHz
- 12-bit resolution
- Up to 11 external analog input channels: ADC1/2/3/4/5/6/10/12/13/14/15
- Four internal dedicated channels:
  - VBAT monitoring channel, connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - Two internal calibration channels, connected to ADC8/11
- Conversion modes:
  - One-shot mode
  - Continuous mode

## 4.24 Timer Groups (TIMG)

The BK7259 includes four general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

## 4.25 Watchdog Timers (WDT)

The BK7259 has one watchdog timer in the AON power domain and one window watchdog timer in each CPU core. The purpose of the watchdog timers is to detect and recover from failures or malfunctions.

### 4.25.1 AON Watchdog Timer (AWDT)

The AON power domain watchdog timer (AWDT) is based on a 16-bit up-counter. It runs on the ROSC and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds. The AWDT triggers a reset on expiry of a programmed time period.

### 4.25.2 CPU Window Watchdog Timers (WWDT)

Each CPU core has a window watchdog timer (WWDT). Each window watchdog timer is based on a 16-bit up-counter. It is clocked from the LPO_CLK clock. The WWDT trigger a reset on expiry of a specified time period. A reset is also generated if the down-counter is reloaded outside the window.

## 4.26 Real-time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

## 4.27 IrDA Interface (IRDA)

The BK7259 embeds a hardware IrDA interface that supports waveform analysis and waveform generation. The IrDA interface monitors the start of infrared signals, records the sequence of infrared waveforms, stores the waveforms in the RX FIFO for software analysis, and writes the waveforms to be sent to the TX FIFO when sending, thereby enabling the analysis and transmission of any infrared protocol.

The IrDA interface has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

## 4.28 Temperature Sensor

The BK7259 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

# 5. Package Information

**Figure 5-1 QFN128 12.3 x 12.3 mm Package Outline**

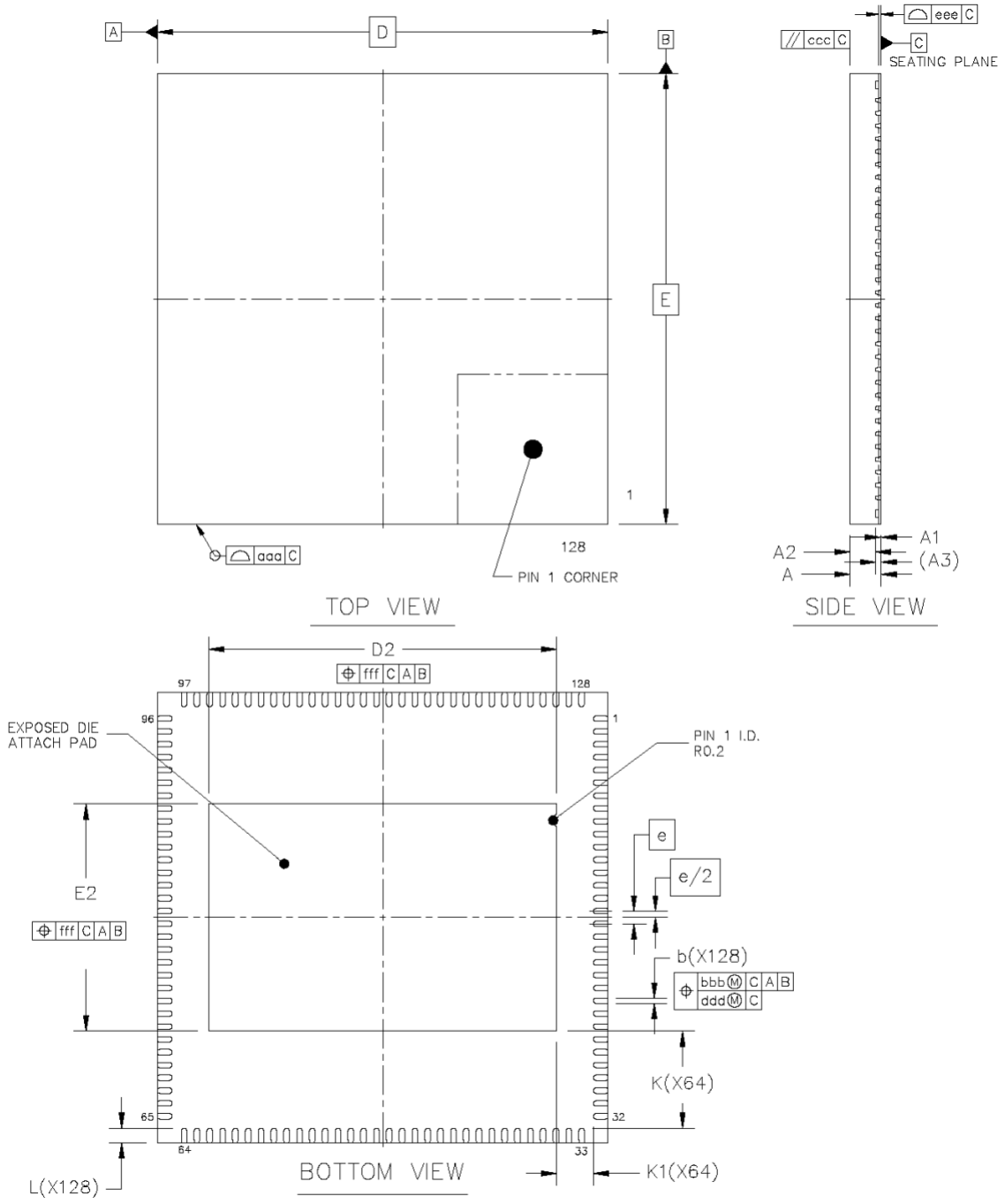
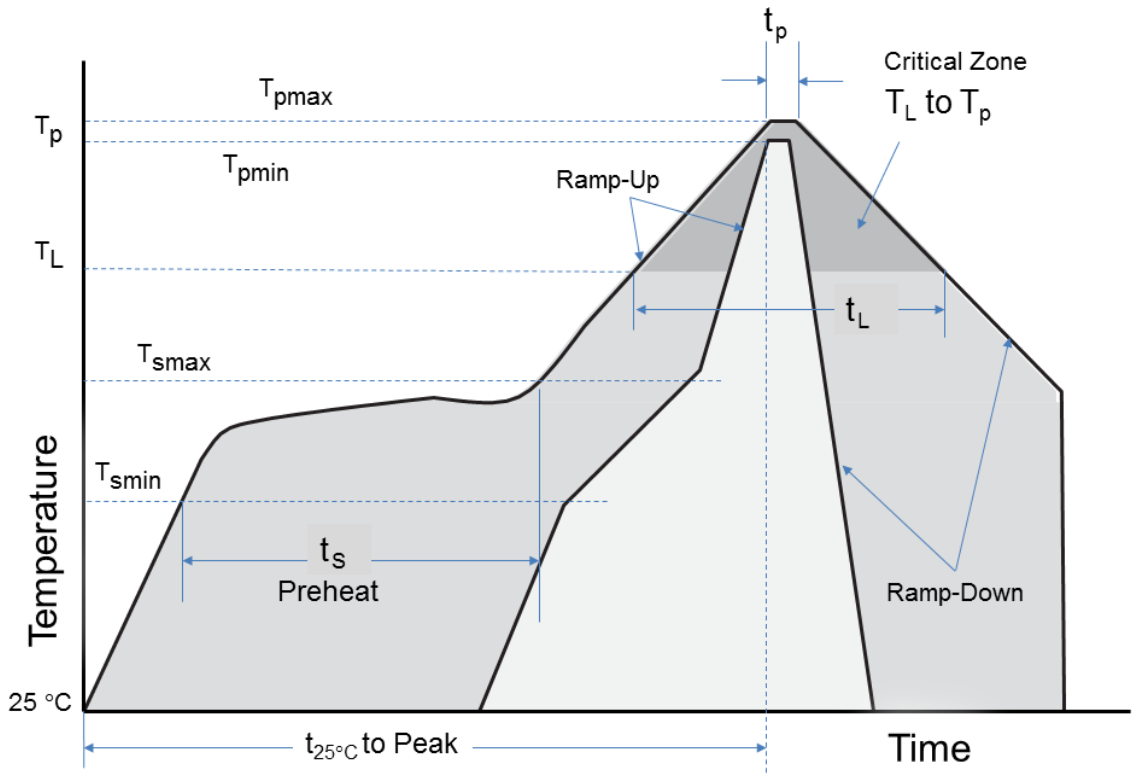


**Table 5-1 QFN128 Package Dimensions**

| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | - | 0.70 | - |
| A3 | 0.152 REF | | |
| b | 0.10 | 0.15 | 0.20 |
| D | 12.30 BSC | | |
| E | 12.30 BSC | | |
| e | 0.35 BSC | | |
| D2 | 9.40 | 9.50 | 9.60 |
| E2 | 6.10 | 6.20 | 6.30 |
| L | 0.30 | 0.40 | 0.50 |
| K | 2.65 REF | | |
| K1 | 1.00 REF | | |
| aaa | 0.10 | | |
| ccc | 0.10 | | |
| eee | 0.08 | | |
| bbb | 0.07 | | |
| ddd | 0.05 | | |
| fff | 0.10 | | |

# 6. Reflow Soldering Profile

**Figure 6-1 Reflow Soldering Profile**




| Profile Feature | | Specification |
|---|---|---|
| Average ramp-up rate ($T_{smax}$ to $T_p$) | | 3 °C/s max. |
| Preheat | Temperature min. ($T_{smin}$) | 150 °C |
| | Temperature max. ($T_{smax}$) | 200 °C |
| | Time ($t_s$) | 60 s to 180 s |
| Time maintained above | Temperature ($T_L$) | 217 °C |
| | Time ($t_L$) | 60 s to 150 s |
| Peak/classification temperature ($T_p$) | | 260 °C |
| Time within 5 °C of actual peak temperature ($t_p$) | | 20 s to 40 s |

| Profile Feature | Specification |
| --- | --- |
| Ramp-down rate | 6 °C/s max. |
| Time 25 °C to peak temperature | 8 minutes max. |

## RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

## ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

## Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

# 7. Ordering Information

**Figure 7-1 Ordering Code Scheme**

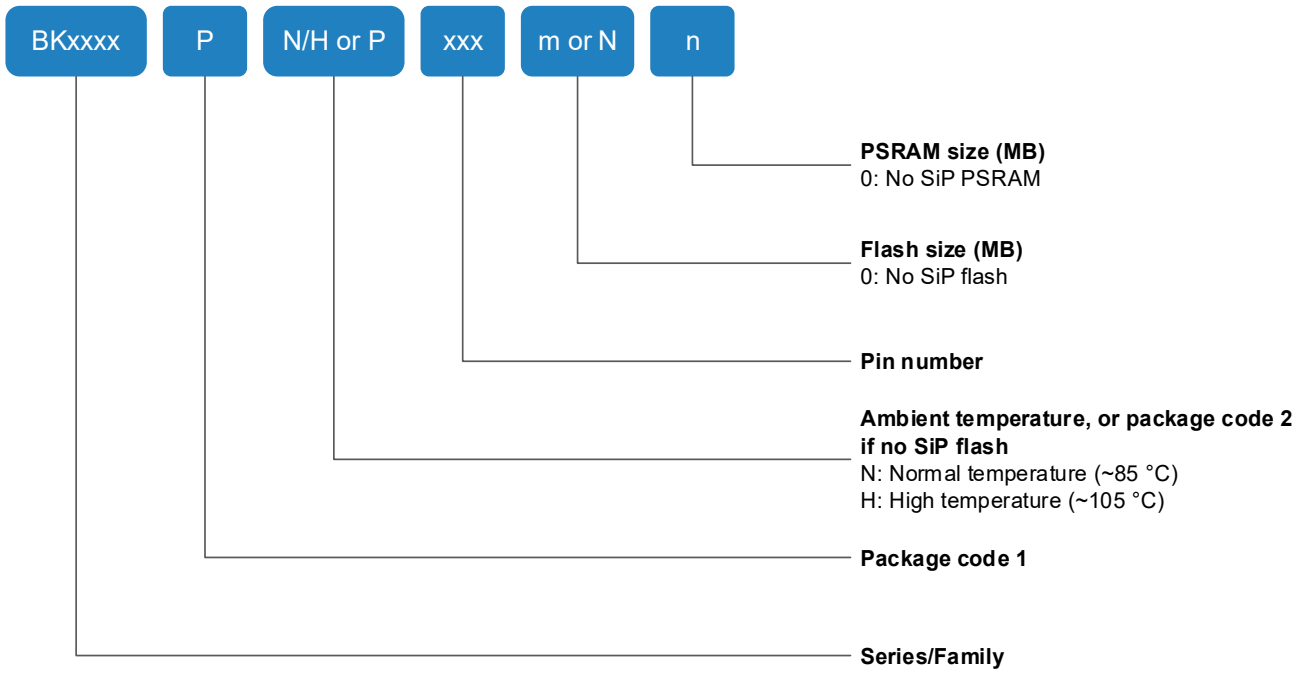



**Table 7-1 Ordering Information**

| Ordering Code | Package | SiP Flash(1) | SiP PSRAM(1) | Packing | Minimum Ordering Qty (MOQ) |
|---|---|---|---|---|---|
| BK7259QN128832 | 12.3 mm x 12.3 mm QFN128 | 8 MB | 32 MB | Tape and Reel | 3000 |

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

# Revision History

| Version | Date | Description |
|---|---|---|
| 1.0 | 2024/11/8 | Initial release |
| 1.1 | 2025/2/14 | • Changed Bluetooth LE support to dual-mode Bluetooth support<br>• Updated the maximum resolution of the ISP in Section 4.21.5 Image Signal Processor (ISP)<br>• Updated the ordering code scheme in Section 7 Ordering Information: 0 means no SiP flash |

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